WE CLAIM:

1. A semiconductor device comprising:

a semiconductor chip having an active and a passive surface, said active surface including an integrated circuit (I/C) and input/output (I/O) pads suitable for metallurgical contacts; and

a protective plastic film of controlled and uniform thickness selectively attached to said passive surface, said film suitable to absorb light of visible and infrared wavelengths, to remain insensitive to moisture absorption, and to exert thermomechanical stress on said chip such that said stress at least partially neutralizes the stress exerted by an outside part after chip assembly.

2. The device according to Claim 1 wherein said light absorption is more than 96 % for all wavelengths.

3. The device according to Claim 1 wherein said neutralizing stress is provided by a film selected for suitable thickness and a coefficient of thermal expansion (CTE) approximately matching the CTE of said outside part.

4. The device according to Claim 3 wherein said film thickness is in the range from 20 to 100 μm.

5. The device according to Claim 3 wherein said film has a CTE between about 18 and 45 ppm/°C and a flexural modulus of about 16 GPa.

6. The device according to Claim 1 wherein said film is attached to said chip with an adhesion strength of about 400 kg/cm^2 after curing.

7. The device according to Claim 1 wherein said moisture absorption is about 0.85 weight %.

8. The device according to Claim 1 wherein said plastic film is selected from a group of electrically insulating materials consisting of polyimide, epoxy resin, and silicone, and said film further including hardener, tackyfier, and fillers.

9. The device according to Claim 8 wherein said hardener is about 4 % amine type.

10. The device according to Claim 8 wherein said tackyfier is about 5 % thermoplastic resin.

11. The device according to Claim 8 wherein said fillers include 50 to 60 % larger particle size silica, and 12 to 15 % smaller particle size silica.

12. The device according to Claim 1 wherein said film further can be marked by laser or ink inscribing.

13. The device according to Claim 1 wherein said I/O pads on said active chip surface are configured in proximity to the stress-neutral central chip portion and distant from the stress-maximum peripheral portions.

14. The device according to Claim 1 wherein said I/O pads have a metallization suitable for attachment to outside parts either by forming welds under thermocompression bonding, or solder connections under reflow conditions, or adhesive connections under adhesive attachment.

15. An assembly of a semiconductor device onto an outside part comprising:

a semiconductor chip having active and passive surfaces, said active surface including an I/C and I/O pads suitable for metallurgical contacts;

a protective plastic film of controlled and uniform thickness selectively attached to said passive

surface, said film suitable to absorb light of visible and infrared wavelengths, to remain insensitive to moisture absorption, and to exert thermomechanical stress on said chip such that said stress at least partially neutralizes the stress exerted by an outside part after chip assembly;

an outside part, integral with electrically conductive interconnection lines in an insulating body and metallized terminals aligned with said chip I/O pads; and

said chip I/O pads electrically connected to said aligned metallized terminals of said outside part.

16. The assembly according to Claim 15 wherein said electrical connection is selected from a group of techniques and materials comprising:

direct welding by metallic interdiffusion;

attachment by solder paste; and

attachment by conductive adhesive.

17. The assembly according to Claim 15 wherein said outside part is an assembly board selected from a group of organic material including FR-4, FR-5, and BT resin, with or without strengthening or thermally modulating fibers; metals; and ceramics.

18. The assembly according to Claim 17 wherein the CTE of said outside part is selected to be approximately matching the CTE of said plastic film.

19. A method for completing the fabrication of a semiconductor device, comprising the steps of:

providing a semiconductor wafer having an active and

a passive surface, said active surface including a plurality of chips having I/Cs and I/O pads suitable for metallurgical contacts;

providing a suitable length of adhesive plastic film of controlled and uniform thickness, said film suitable to absorb light of visible and infra-red wavelengths, to remain insensitive to moisture absorption, and to exert thermomechanical stress on said chips such that said stress at least partially neutralizes the stress exerted by an outside part after chip assembly;

rolling said film onto said passive wafer surface;

curing said film at elevated temperatures for a length of time sufficient to increase the adhesion strength between said film and said wafer to a predetermined value; and

singulating said chips by sawing said wafer through said semiconductor and said adhering film.

20. The method according to Claim 19 wherein said curing comprises a temperature of about 150 °C and a length of time of about 1.0 hr.